Institute of Business & Information Technology
University of the Punjab
Quaid-e-Azam Campus, Lahore

Spring Term

Basic Information:

Title:	Computer Architecture	**Code**	IT 463
Program:	BBIT (Major in Information Technology)	**Credit Hours:**	Three (03)
Sessions:	30 Classes + Mid Term + Final Term	**Pre-Requisite:**	IT 162

Course Description:

The course of computer architecture is concerned with the structure and behavior of the various functional modules of computer and how the interact to provide the processing needs of the user. To write high-performance computer programs, it is essential to know the underlying hardware on which those programs will execute. Major part of this course will focus on architectures and memory systems. Today's computer hardware sector faces significant challenges. The multi-core revolution is at the heart of these challenges. The shift from single processor models to multi-core design needs knowledgeable hardware and software designers about a variety of problems including hardware in parallel computing.

Learning Outcomes:

After the completion of this course, it is expected that students who will involve themselves in the knowledge base working of the course will be capable to

1. *Understand the design of a pipelined CPU and cache hierarchy*
2. *Analyze and evaluate CPU and memory hierarchy performance*
3. *Understand hardware design of multiprocessors including cache coherence and synchronization*
4. *Experience with a complex simulation tool to study various microarchitectural features.*

Teaching Learning Methodology:

The formal teaching component of this course consists of active student participation in and contribution to all forms of teaching and learning i.e. lectures, discussions, research assignments and projects. Lectures will be twice a week of 90 min each.

Group Configurations:

One of the objectives of this course is to encourage and facilitate teamwork. Class will have to make a group of four for projects and research assignments. It is recommended that student will form their own groups. As a general guideline, your group should have members with diverse skill sets including people who are proficient or have aptitude for different subject areas.

Weekly Term Plan

Wk	Lecture Topic	Activity
01	*Computer Organization Basics*	
02	*RTL, Microoperations, Design of Arithmetic Microoperations*	*A01*
03	*Logic Microoperations, Design of Buses*	*Quiz 1*
04	*Basic Computer Organization and Design*	
05	*Timing and Control, Instruction Cycle*	*A02*
06	*Register Reference Instructions,*	*Quiz 2*
07	*Design Of ALU, General Register Organization*	
08	*Mid Term Examination*	
09	*RISC And CISC Architectures, Introduction to Pipelining*	
10	*Arithmetic Pipeline, Instruction Pipeline, Hazards, Handling of Hazards*	
11	*Dynamic Branch Prediction*	*A03 & Quiz 3*
12	*Limitations to Instruction Level Parallelism (ILP) and Thread Level Parallelism*	
13	*Simultaneous Multi-Threading (SMT)*	*A04*
14	*Memory Hierarchy, Main Memory, Associative Memory*	*Quiz 4*
15	*Cache Memory and Mapping Techniques*	
16	*Final Term Examination*	

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Topics in Detail

Introduction
- *Review of Logic Design*
- *Computer Organization Basics*

Basic Computer Organization and Design
- *Instruction Codes*
- *Timing and Control*
- *Instruction Cycle*
- *Memory Reference Instructions*
- *Input-Output and Interrupt*
- *Design of Basic Computer*
- *Design of Accumulator Logic*

Register Transfer
- *Register Transfer Language*
- *Three State Bus Buffers*
- *Memory Transfer*

Microoperations
- *Design of Arithmetic Microoperations*
- *Binary Adder*
- *Binary Adder-Subtractor*
- *Binary Incrementor*
- *Arithmetic Circuit*
- *Logic Microoperations*
  - *Hardware Implementation*
- *Shift Microoperations*
  - *Hardware Implementation*
- *Arithmetic Logic Shift Unit*

Central Processing Unit
- *Register Organization*
- *Stack Organization*
- *Instructions Format*
- *Addressing Modes*
- *Data Transfer and Manipulation*
- *Program Control*
- *RISC*

Pipeline and Vector Processing
- *Parallel Processing*
- *Pipelining*
- *Arithmetic Pipelining*
- *Instruction Pipelining*
- *RISC Pipeline*
- *Pipelining Hazards*
- *Handling Hazards*
- *Branch Prediction*

Instruction Level Parallelism
Thread Level Parallelism
Simultaneous Multi-Threading

Memory Organization
- *Main Memory*
- *Auxiliary Memory*
- *Associative Memory*
- *Virtual Memory*
- *Cache Memory*
- *Memory Mapping Techniques*
- *Memory Management Hardware*

Text & Recommended Readings

A. *Computer System Architecture by Morris Mano*

B. *Computer Organization and Design by Hennessy and Patterson*

Assignment Specification

1. *Microsoft Word for Documentation*

Headings	*Arial 11pt Bold*
Normal Text	*Times New Roman 10pt*
Header Footer	*Times New Roman 8pt*
Paragraph	*Single Line Spacing*
	First Line Indent 1.0 cm
Page Margins	*2 cm from each side*

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Grading Policy:

Final Grade for this course will be the cumulated result of the following term work with relevant participation according to the quoted percentage.

Sessional	**25%**		***Mid Term***	**35%**		***Final Term***	**40%**
Assignments	10 %		*Mid Term Exam*	25%		*Final Exam*	30%
Quizzes	10%		*Major Report/Work*	10%		*Case Study/ Project/ Term Paper*	10%
Presentations	05%						

Remember subdivision of Mid Term and Final Term Examination should be done only in extreme cases of very essential and major Grading Instruments.

Dishonest Practices & Plagiarism

Any student found responsible for dishonest practice/cheating (e.g. copying the work of others, use of unauthorized material in Grading Instruments) in relation to any piece of Grading Instrument will face penalties like deduction of marks, grade 'F' in the course, or in extreme cases, suspension and rustication from IBIT.
For details consult Plagiarism Policy of PU at http://pu.edu.pk/dpcc/downloads/Plagiarism-Policy.pdf

Grading System:

Letter Grade	Grade Point	Num Equivalence
A	4.00	85 – 100 %
A-	3.70	80 – 84 %
B+	3.30	75 – 79%
B	3.00	70 – 74 %
B-	2.70	65 – 69 %
C+	2.30	61 – 64 %
C	2.00	58 – 60 %
C-	1.70	55 – 57 %
D	1.00	50 – 54 %
F	0.00	Below 50 %
I	Incomplete	*
W	Withdraw	*

Norms to Course:

- ✓ *Submission Date and Time for the term instruments is always* **Un-Extendable**
- ✓ *5 Absentees in class will result in forced withdrawal.* ***(PU Policy)***
- ✓ *Re-sit in Mid and Final Term will cause you a loss of 2 and 3 grade marks respectively.* ***(PU Policy)***
- ✓ *This is your responsibility to keep track of your position in class evaluation units.*
- ✓ *After the submission date, NO excuse will be entertained.*
- ✓ ***Keep a copy of all submitted Grading Instruments.***
- ✓ *Assignment is acceptable only in its Entirety.*
- ✓ *No make up for any assignment and quiz.*
- ✓ *Copied & Shared work will score Zero.*
- ✓ *Assignments are Individual.*

Good Luck

For the Spring Term